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PG Semester III

Paper - CC-12

unit - 5

Topic - Synchronous counters

and counter reset itself. It may be remembered that such a reset condition is achieved only after the application of 16th pulse in a scale of 16 counter.

Synchronous counters

Refer to 4-bit ripple counter in fig 1(b) to the input after the seventh pulse. Outputs Q_A, Q_B and Q_C are high. When eighth input pulse is applied, Q_A goes from high to low. This causes Q_B to go from high to low. which causes Q_C to go from high to low. Thus falling edge of eighth pulse causes a transition in each of the succeeding flip flops, the effect rippling through the counter. Thus clock pulse effectively ripples through the chain of flip flops. It causes carry propagation delay (which is the time for a counter to complete its response to an input pulse) because any flip flop will not respond unless the preceding flip flop has completed its transition. Therefore, when the output of one flip flop drives another, the counter is called a ripple counter. FF/A has to change states before it can trigger the FF/B flip flop, FF/B has to change before it can trigger

FF/C and so forth. The triggers move time is the sum of the individual delays. If each flip flop in a 4-bit binary counter has a t_p of 10 ns, the overall propagation delay will be equal to 40 ns. Propagation delay time can be reduced considerably in synchronous counter in which all flip flops are controlled by a common clock. There are two methods of flip flops control in synchronous counters:

(i) with ripple (or series) carry, and

(ii) with parallel carry (or carry look ahead).

The latter is the faster of the two methods.

(A) 5-Bit Synchronous Counter with series carry:

Refer to fig (3)(a). Each flip flop is a T-type. The connections to be made to T-inputs are deduced from waveform chart of fig 3(b). The positive going shift pulses have been considered. The state of FF A will cange with each pulse, i.e. flip flop

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toggles from one state to another at each clock pulse. Thus

Q_A toggles with each clock pulse,

$T_A = 1$

Q_B complements only if $Q_A = 1$, $T_B = Q_A$

Q_C becomes $\bar{Q}_C$ only if $Q_A = Q_B = 1$, $T_C = Q_A Q_B = T_B Q_B$

Q_D toggles only if $Q_A = Q_B = Q_C = 1$, $T_D = Q_A Q_B Q_C = T_C Q_C$

Q_E toggles only if $Q_A = Q_B = Q_C = Q_D = 1$, $T_E = Q_A Q_B Q_C Q_D = T_D Q_D$

To perform this logic (e.g. $Q_C \rightarrow \bar{Q}_C$ if $Q_A = Q_B = 1$) two input AND gates are used (fig 3a).

Since the carry passes through all the control gates, this is a Synchronous counter with series carry (or ripple carry). In fig 3(b) all 16 states of the counter are shown.

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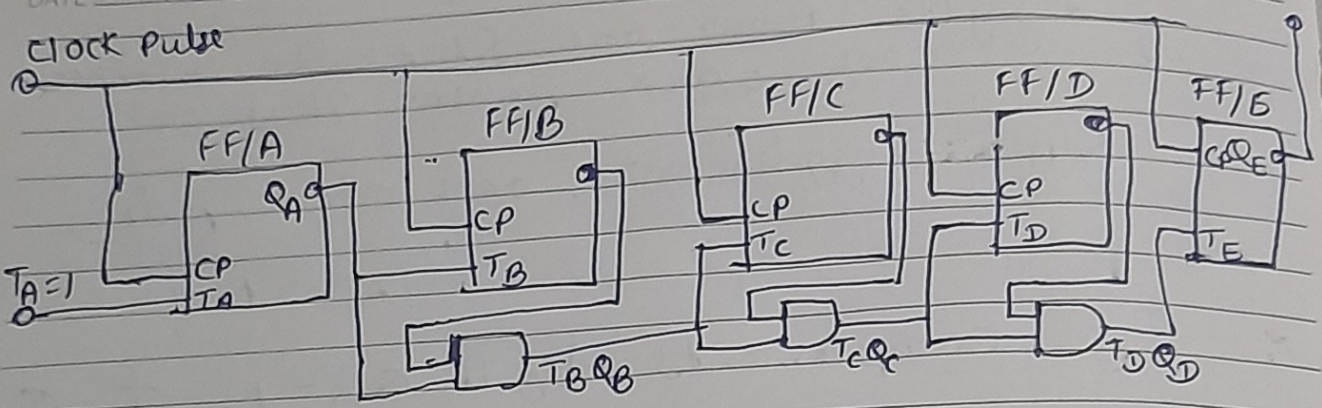

fig 3(a) A 5-bit Synchronous counter with series carry ($J = K = T$)

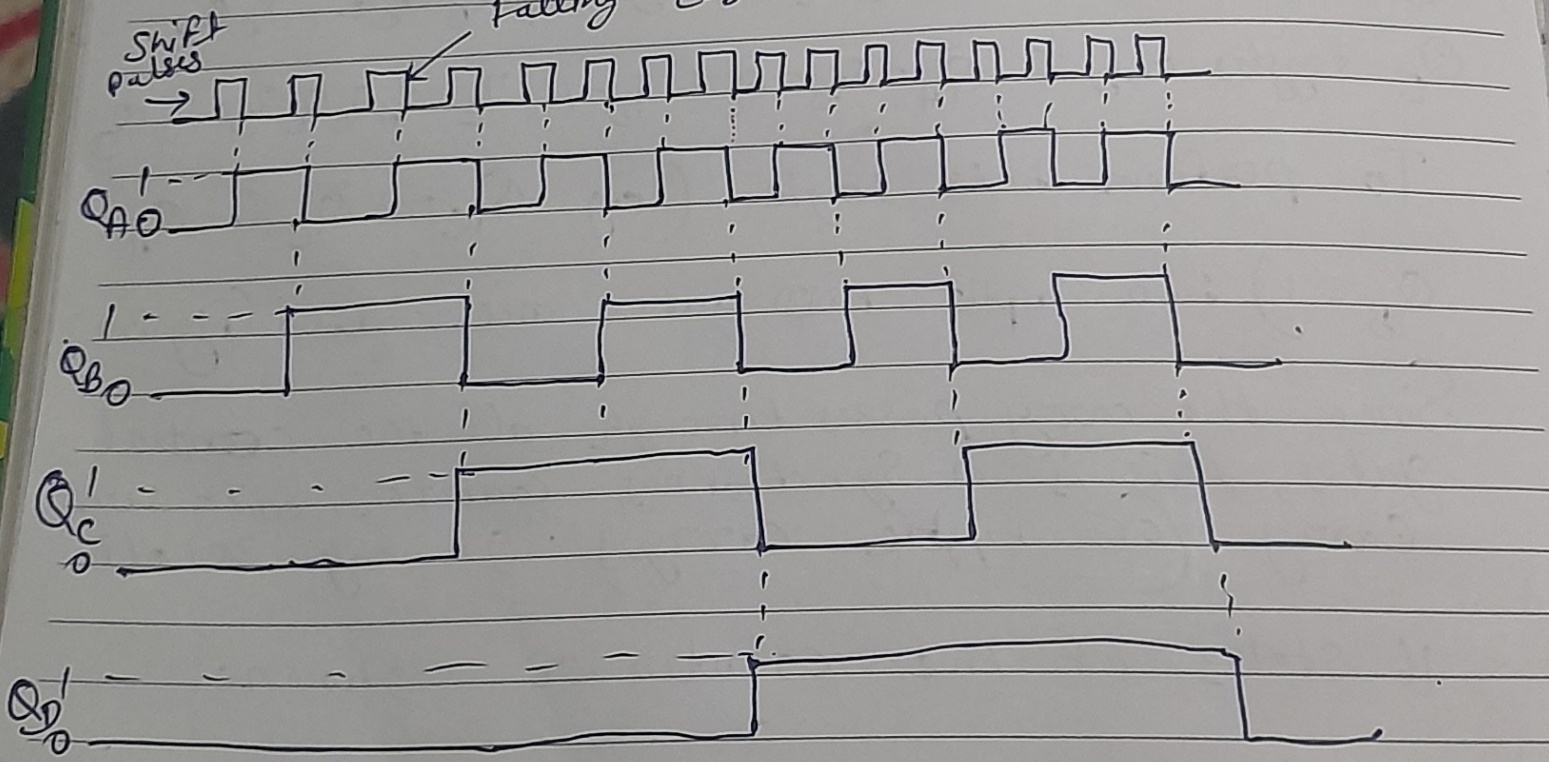

fig 3(b) Waveform chart

Number of input Pulses	Flip flop outputs			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

fig 3① States of FF